Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **Q12**
2. **Q6**
3. **Q5**
4. **Q7**
5. **Q4**
6. **Q3**
7. **Q2**
8. **VSS**
9. **Q1**
10. **C**
11. **R**
12. **Q9**
13. **Q8**
14. **Q10**
15. **Q11**
16. **VDD**

**.069”**

**.079”**

**10 9 8 7**

**15 16 1 2**

**6**

**5**

**4**

**3**

**11**

**12**

**13**

**14**

**DIE ID**

**CD4040BA**

**Top Material: Al**

**Backside Material: SiNi**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VDD**

**Mask Ref: CD4040BA**

**APPROVED BY: DK DIE SIZE .069” X .079” DATE: 10/20/21**

**MFG: TEXAS / HARRIS THICKNESS .025” P/N: CD4040BH**

**DG 10.1.2**

#### Rev B, 7/19/02